

ABSTRACT

A printed circuit board having contacts in a contact array of rows and columns. Groups of n columns of the contacts are electrically connected to $n-1$ columns of vias disposed interstitially in a via array between the n columns of the contacts. A major vertical routing channel is formed between adjacent groups of n columns of the contacts and the $n-1$ columns of vias. First electrical traces are electrically connected to a first number of the vias. The first electrical traces are routed to an outside edge of the via array through the major vertical routing channel.

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